```
 CCCCCCCC     TTTTTTTTTTTT      CCCCCCCC
CC       CC         TT         CC       CC
CC       CC         TT         CC       CC
CC                  TT         CC
CC                  TT         CC
CC                  TT         CC
CC                  TT         CC
CC                  TT         CC
CC       CC         TT         CC       CC
CC       CC         TT         CC       CC
 CCCCCCCC           TT          CCCCCCCC
```

CARTRIDGE TAPE CONTROLLER

AN ALPHABETICAL LISTING OF THE SIGNAL MNEMONICS USED ON THE CTC SCHEMATICS

P.C. Board Rev..... C
DATE ..... Oct. 13th, 1981

This document should contain everything you need to help you decipher the schematics.

Written by

David W. Milton

ON ALL BUSSES IN THE CTC AND ANY OTHER PLACES, BIT 0 IS ALWAYS THE LSB.

6.1MHZ This is the approximate rate the VCO runs at when following low density MFM data.

7.9MHZ This is the approximate rate the VCO runs at when following high density GCR data.

ACE+ A.C. ERASE. This signal is part of the logic to write A.C. erased inter-record gap onto the tape.

AE A.C. ERASE. This is an instruction to the write logic to write an A.C. erased inter-record gap.

BIT+ BIT. If sampled on the falling edge of BIT CLK-, this is the state of the bit just decoded off the tape.

BITCLK- BIT CLOCK. This is a signal whose falling edge says now is the time to sample the bit decoded off the tape which is the signal "BIT+".

BITTMO+ BIT TIME. A signal within the read logic. A pulse here delimits the bit cells so the bit can be recorded and counted.

BOT+ BEGINNING OF TAPE. Status from the selected drive indicating the installed tape cartridge is at BOT.

BOTW+ BEGINNING OF TAPE WARNING. Status from the selected drive indicating the installed tape cartridge is near BOT.

BPT- BREAKPOINT. A signal from the debugger which will stop the CTC's clocks exactly like STP- does, in the 3rd quarter of the instruction.

BT- BEGINNING OF TAPE. An intermediate signal indicating the selected drive's tape cartridge is at BOT.

BUS OK- BUS OKAY. This is the signal to the drive to idicate power is good so the commands it is receiving are real.

BW- BEGINNING OF TAPE WARNING. An intermediate signal indicating the selected drive's tape is near the beginning.

C5-C0	CONDITION SELECT. These bits specify what condition to save for the next instruction to see as "CX-".
C7	CRC-7. This is an instruction to the write logic to write 7 bits this time instead of 8. This is used to write the second half of the 15 bit CRC used on MFM records.
CCI+	COMMAND-COMMAND-IN. This condition is the state of one of the handshake signals to communicate with the PPU.
CCO+	COMMAND-COMMAND-OUT. This condition is the state of one of the handshake signals to communicate with the PPU.
CFI+	COMMAND-FLAG-IN. This condition is the state of one of the handshake signals to communicate with the PPU.
CFO+	COMMAND-FLAG-OUT. This condition is the state of one of the handshake signals to communicate with the PPU.
CHCRC+	CHECK CRC. This is SYNCHK+ before it is sysnchronized to the byte counter. It turns on the error latching circuit.
CI	CARRY-IN. The micro-instruction specifies the carry-in to the ALU. This signal is active high.
CLK+	CLOCK. This is exactly (in time) CLK5-1- inverted. Its falling edge delimits the micro-instruction.
CLK5-1-	CLOCKS, 5 thru 1. The rising edge is the next instrucion clock, and these control most of this synchronous machine.
CO+	CARRY-OUT. This condition is the carry-out of the most significant bit of the ALU.
CRC+	CRC ERROR. This condition latches to indicate the data CRC did not match the expected one.
CRC7+	CRC-7. This signal in the write logic makes the control PROM unpak only 7 bits to be written to the tape rather than 8. It is used to write MFM's 15 bit CRC.
CRINIT-	CRC INITIALIZE. This signal resets and holds reset the CRC checking, error latching register.
CRST-	CRC RESET. A signal in the read logic to reset the CRC checking circuit.
CSD-	CONTROL STORE DISABLE. A signal from the debugger which disables the control store PROMS on board the CTC.
CX-	CONDITION. This is the state of the condition specified in the previous micro-instruction. Low is true.

D7-D0 DATA BUS. This is the CTC's main data bus. It appears almost everywhere in the schematics. Bit 0 is the LSB.

DCI+ DATA-COMMAND-IN. This condition is the state of one of the handshake signals to communicate with the PPU.

DCO+ DATA-COMMAND-OUT. This condition is the state of one of the handshake signals to communicate with the PPU.

DCO+DFI This signal is the inverted OR of Data-command-out and Data-flag-in. It is labeled because it aslo appears on page 1 of these schematics as the enable on un-used gates.

DDA+ DATA DETECTED. Half of the differential pair which indicate valid flux transitions are being read off the tape now.

DDA- DATA DETECTED. Half of the differential pair which indicate valid flux transitions are being read off the tape now.

DDB- DISPLAY DATA BUS. A signal from the debugger which enables the CTC data bus out J6 pins 0-7.

DELAYED ACE. This is the signal "ACE" (A.C. erase) delayed in time by three bit cell.

DFI+ DATA-FLAG-IN. This condition is the state of one of the handshake signals to communicate with the PPU.

DFO+ DATA-FLAG-OUT. This condition is the state of one of the handshake signals to communicate with the PPU.

DPE+ DATA PARITY ERROR. If checked at the right time, this condition indicates an error on data coming from the PPU.

DR+ DRIVE READY. An intermediate signal indicating the selected drive is working and has a tape installed.

DR1+DR0+ DRIVE SELECT. Intermediate signals to select one of four drives on the daisy chain. Drive 00 is the first one.

DR1-DR0- DRIVE SELECT. These two lines select one of four drives on the daisy chain. Drive 11 is the first drive on the chain.

DRDY- DRIVE READY. Status from the selected drive indicating the drive is working and has a tape installed.

DWCRC+ DELAYED WRITE CRC. This is WCRC+ delayed by one byte time, which is 8 or 7 bit times, depending on CRC7.

E7-E0- ENABLES, 7 thru 0. These are the enables to enable registers onto the data bus, or sometimes to clear a register.

EBC+ ENABLE BYTE COUNTER. A signal in the read logic to enable the byte counter to increment and to reset the bit counter.

EBC- ENABLE BYTE COUNT. This is EBC+ inverted.

END BIT CELL+. This is a pulse to mark the end of a bit cell and reset the data decoder in the read logic to zero.

ENWD+ ENABLE WRITE DATA. This signal enables the WDR and WDL signals to flag control of data being fed to the write logic.

EOT+ END OF TAPE. Status from the selected drive indicating the installed tape cartridge is at EOT.

EOTW+ END OF TAPE WARNING. Status from the selected drive indicating the installed tape cartridge is near EOT.

ERD+ ENABLE READ DATA. This enables SRQ+ to set RDR and RDL and let the read logic communicate with the micro-code.

ET- END OF TAPE. An intermediate signal indicating the selected drive's tape is at EOT.

EW- END OF TAPE WARNING. An intermediate signal indicatng the selected drive's tape is near EOT.

F4-F0 FROM, 4 thru 0. These 5 bits specify the source of the data on the data bus and usually the "A" input to the ALU.

FW+ FORWARD. An intermediate signal to tell the drive to move the tape forwards.

FWD- FORWARD. This is the signal to the drive to tell it to move the tape forwards.

HDEN+ HIGH DENSITY. The CTC loads a register to indicate the recording density is high (GCR) or low (MFM).

HDEN- HIGH DENSITY. This is the above signal inverted.

HS+ HIGH SPEED. An intermediate signal to tell the drive to move the tape at 90ips rather than 30 inches per second.

HSP- HIGH SPEED. This is the signal to the drive to tell it to move the tape at 90ips rather than 30 inches per second.

I8-I0 INSTRUCTION, 8 thru 0. These 9 bits specify the ALU operation to be performed in this instruction.

ID1-ID0- IDENTIFICATION. These signal are the identity number for the first drive on the daisy chain. Since these are both tied high on the CTC, that means when DR0- and DR1- = 11, the selected drive will be the first on on the daisy chain. If you wanted the daisy chain to have first drive 1, then 2, 3, and 0, you would want ID1-,ID0- = 1,0 because then DR1-,DR0- = 1,0 would select the first drive on the daisy chain. This is drive one because DR1+,DR0+ = 01 !

IDLE+ IDLE. This is IDLE- inverted.

IDLE- IDLE. The read logic is idle and instructing the phase lock loop to track TB4, which is the nominal data rate.

J10-J0 JUMP ADDRESS. This is the 11 bit jump address field in micro-control store as it comes out of the input registers.

JX3-JX0 JUMP ADDRESS INDEXED. The 4 LSB's of the jump address field may be replaced by the 4 LSB's of the previous instruction's data bus.

LC-L0- LOAD STOBES, #C thru 0. These are the load strobes used in the CTC to load the data bus into registers, or sometimes to clear a register.

LBC- LOAD BYTE COUNTER. A signal in the read logic to load a new byte count from the jump table PROM into the byte counter.

LDATA+ LOAD DATA. This is LDATA- inverted.

LDATA- LOAD DATA. A control signal in the write logic to transfer data from the Write Data register to the bit unpak-er.

LDBYTE+ LOAD BYTE. This is LDBYTE- inverted.

LDBYTE- LOAD BYTE. The write logic unpaks bytes and nibbles into bits. This is one of the signals to do that. See Write Control PROM timing diagram for details.

LDEN+ LOW DENSITY. The CTC loads a register to indicate the recording density. This is HDEN+ inverted.

LDN+ LOAD NIBBLE. A signal in the read logic used to re-pack the bits into nibbles for GCR decoding. See FPLA timing diagram for details.

LDNIB- LOAD NIBBLE. The write logic unpaks bytes and nibbles into bits. This is one of the signals to do that. See Write Control PROM timing diagram for details.

LOCK+ LOCK. The read logic has determined the phase lock loop is synchronized with the data and instructs the phase lock loop to stay locked onto the data's phase rather than its frequency.

MFM WINDOW+. If a Read Data Transition occurs in this half of the MFM bit cell, the bit-cell cntains a "1" bit.

N+2
N+1
N
N-1
N-2

These 5 signals are a snap-shot of 5 bits which are being written onto the tape, the middle one (N) which is the one being written now. The Pre-stress and Equalization PROM looks at these 5 bits and shifts the middle one in time a little bit before actually writing it. N+1 will be written next, N-1 was written last.

OV+ OVERFLOW. This condition indicats the ALU output has overflowed into the sign bit if you are doing 2's compliment arithemetic.

PD- PUMP DOWN. An instruction to the charge pump to lower the conrol voltage to the VCO and slow it down.

PFW- POWER FAIL WARNING. This signal comes from the PPU and originally the SSU to warn of impending system reset or power loss.

PLLCLK PHASE LOCK LOOP CLOCK. This is the output of the VCO which runs at 32 times the data frequency which the PLL is following.

PN- POWER ON. This is active low to indicate power is okay. It is derived from PON+ and goes to the drives as BUS OK-.

PON+ POWER ON. When high, the RESET signal from the PPU is inactive and the CTC's +5 volts is at least 4.9 volts.

PU- PUMP UP. An instruction to the charge pump to raise the control voltage to the VCO and speed it up.

PW+ POWER WARNING. This condition indicates the POWER FAIL WARNING signal from the PPU is active.

RA9-RA0 RAM ADDRESS. These 10 bits address the 1Kx8 of on board RAM. There are 2 sources for the RAM address. Bit 0 is the LSB.

RAD- ROM ADDRESS DISABLE. A signal from the debugger which disables the CTC's control-store PROM address drivers.

RCRC- RESET CRC. This signal is timed correctly to clear the CRC generator at the correct time in the write timing sequence.

RCRC7+ READ CRC 7. This signal instructs the read logic to read 7 more bits instead of 8. It is used to read the second half of the MFM 15 bit CRC.

RCW- RESET CRC WRITE. This signal instructs the write logic to clear (zero out) the CRC generator.

RDA+ READ DATA. Half of the differential pair which are the flux transitions which are being read off the tape now.

RDA- READ DATA. Half of the differential pair which are the flux transitions which are being read off the tape now.

RDD+ READ DATA DETECTED. This condition indicates valid flux transitions are being detected by the drive.

RDL+ READ DATA LATE. This condition latches to indicate the read logic was not serviced on time and wrong data will be read.

RDR+ READ DATA READY. This condition indicates it is time to read a byte of data from the read logc.

RDX+ RDD CHANGED. This signal latches to indicates "RDD" has changed, if only a glitch, since RDX- was last cleared.

READ DATA TRANSITION-. This is a pulse to represent a syncronized and filtered flux transition which occured on the tape.

REV- REVERSE. This is the signal to the drive to tell it to move the tape in reverse.

RINIT- READ INITIALIZE. This resets and holds reset the signals RDR and RDL.

RST- RESET. This is the state of the RESET signal from the PPU. When low, RESET from the PPU is active.

RTC+ REAL TIME CLOCK. This condition comes true once every 32 or 40 micro-seconds or so, depending on the selected density.

RV+ REVERSE. An intermediate signal to tell the drive to move the tape in reverse.

RVRS+ REVERSE. An unused signal originally intended to tell the read logic it was running the tape backwards. It turned out to be un-necessary.

S3-S0 SELECT NEXT ADDRESS. Micro-control store bits 0:3 are used to select the source of the next micro-address.

SDUM STUPID DUMMY. This was a spare control signal designed in. It is now used to instruct the read logic to find and aquire sync in the next GCR sync zone.

SEL+ SELECT. An intermediate signal to select a drive. It tells the drive whose DR1,DR0 match up to pay attention to the other control signals on the daisy chain.

SEL- SELECT. This is the signal sent out on the daisy chain to tell the selected drive to respond to commands on the daisy chain.

SELD- SELECTED. A response from the selected drive acknowledging that it has been selected.

SF- STACK FULL. This is a condition bit indicating the subroutine return stack is full. Do not push another address onto it.

SHBYTE+ SHIFT BYTE. The write logic unpaks bytes and nibbles into bits. This is one of the signals to do that. See Write Control PROM timing diagram for details.

SHN+ SHIFT NIBBLE. A signal in the read logic used to re-pack the bits into nibbles for GCR decoding. See FPLA timing diagram for details.

SHNIB+ SHIFT NIBBLE. The write logic unpaks bytes and nibbles into bits. This is one of the signals to do that. See Write Control

SHNIB- SHIFT NIBBLE. This is SHNIB+ inverted.

SL+ SELECTED. An intermediate signal indicating the selected drive has acknowledged that it is selected.

SLOK+ SYNCHRONIZE LOCK. This is "LOCK+" before it is syncronized to the byte counter.

SN+ SIGN. This condition is the most significant bit of the ALU output, which is the sign in 2's compliment arithmetic.

SP1&2 SPARE 1&2. Spare signals that never got used.

SRQ+ SET REQUEST. This is a signal in the read logic to set RDR and thus request the micro-code service the read logic.

SS- SINGLE STEP. A signal from the debugger whose falling edge begins 1 micro-instruction when the CTC is stopped.

STB+ STROBE. This is just like CLK1- thru CLK5-, only it is advanced in time by 5 to 9 nano-seconds.

STP- STOP. A signal from the debugger which stops the CTC's clocks when low.

SY SYNC ZONE. This is an instruction to the write logic to write the illegal GCR codes, one of which is the GCR sync zone.

SYNC+ SYNC. This signal instructs the GCR encoder PROM to write illegal codes, one of which is the GCR sync zone.

SYNCHK+ SYNCHRONIZED CHECK CRC. This signal enables the CRC checker to load a latching error flag into a register.

T4-T0 T0, 4 thru 0. These 5 bits specify the data bus destination register and the "B" input/destination in the ALU.

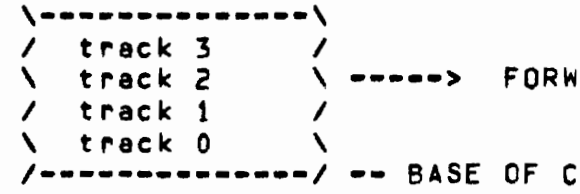
TA7-TA0 TIMING A. These signals divide an 8-bit cell period into 256 parts which the Write Control PROM uses to time the other control signals in the write logic. TA0 is the fastest of these control signals, TA7 is the slowest. See Write Control PROM timing diagram for details.

TB4-TB1 TIMING B. With TA0, these 5 signals divide the bit cell into 32 parts for the Pre-stress PROM to use to move flux transitions around. TB4's period is the nominal bit-cell time and so it is also used as a reference when the Phase Lock Loop is idle-ing. TB4 is the slowest, TA0 the fastest.

TDA+ TAPE DATA AVAILIABLE. This signal indicates that TRD has valid flux transitions rather than just noise.

TR+ TAPE READY. An intermediate signal indicating the selected drive's tape position is known.

TR1-TR0- TRACK 1 thru 0. These two signals go out to the drive to select the appropriate track number.



TR2+TR0+ TRACK 2 thru 0. Three intermediate signals to specify what track to select on the selected drive. Currently there are only 4 tracks to choose from so TR2+ is ignored.

TRD TAPE READ DATA. These are the flux transitions as they are being read off the tape right now.

TRDY- TAPE READY. Status from the selected drive indicating the installed tape's position is known.

WCRC+ WRITE CRC. This signal instructs the write logic to write the bits which are sitting in the CRC generator.

WD WRITE DATA. These are the actual flux transitions which the CTC writes onto the tape.

WDA+ WRIE DATA. This is half of the differential pair which are the flux transitions to be written to the tape.

WDA- WRIE DATA. This is half of the differential pair which are the flux transitions to be written to the tape.

WDL+ WRITE DATA LATE. This condition latches to indicate the write logic was not serviced on time and bad data has been written.

WDR+ WRITE DATA READY. This condition indicates it is time to write another byte of data to the write logic.

WE+ WRITE ENABLE. An intermediate signal to tell the drive to write onto the tape.

WEN- WRITE ENABLE. This is the command to the drive to write to the tape, using both the erase and the write heads.

WINIT- WRITE INITIALIZE. This signal clears and holds clear the WDR and WDL signals.

WP- WRITE PROTECT. An intermediate signal indicating the selected drive has a write protected cartridge installed.

WPT+ WRITE PROTECTED. Status from the selected drive indicating the installed tape cartridge is write protected.

Z+ ZERO. This condition indicates the ALU output is all zero'es. The data bus need not necesarily also be zero.